ARRAY OF INTEGRATED THERMAL SENSORS AND ACTUATORS FOR CRYOBILOGICAL APPLICATIONS

Ajay A. Kardak  
M.S. Candidate

Faculty Advisor: Dr. Ram V. Devireddy

ABSTRACT

Our attempt in this on-going research is to fabricate an integrated device that will fulfill the need by measuring and modulating individual cell temperature [1, 2]. The organization of the proposed device will be an array of 100 (10x10) microscale thermoelectric sensors and actuators. Initially separate arrays of micro thermoelectric sensors, thermocouples, based on seebeck effect [3] and micro thermoelectric actuators, thermoelectric coolers (TEC), based on peltier effect [4] have been fabricated and tested to demonstrate the concepts.

A set of micro thermocouple and a thermoelectric cooler is treated as one unit and the proposed device will have 100, such units. Each device in a single unit is separated by a distance of 11 µm from center-to-center. These units are spaced at a distance of 50µm center-to-center such that the devices can sense and control the temperature of a single cell. As the planar wiring layer at the bottom of the device may act as a heat sink, it can be isolated from the array by using stud bumps. Wiring layer will be fabricated separately on a circuit board. These stud bumps serve as an electrically conducting spacer between the circuit board and the device.

The prototype of the device will be fabricated using multi-step LIGA (Lithographie, Galvanoformung and Abformung) technique. We would incorporate bottom up fabrication process. Fabrication will be done on 4” diameter silicon wafer. First step is to electron beam (e-beam) evaporate 0.01µm titanium adhesion layer and 0.05µm copper plating base to facilitate future electrodeposition steps. A 2µm layer of S1813 resist (Rohm and Haas, Philadelphia, PA) will be spun and baked on the wafer. A UV exposure will performed, resist will be developed, copper will be electro deposited on the micro patterned junction layer recess. A 20µm layer of AZ 4620 (AZ Electronic Materials, Somerville, NJ) was spun, and baked over the top junction layer. An aligned exposure will be made and P-type Bismuth Telluride post will be deposited. A thin layer of S1813 resist will be spun on top to prevent future electrodeposition on already deposited Bismuth Telluride post. N-type Bismuth Telluride, Copper and Constantan post layer will be aligned, exposed and electroplated. A very thin layer of S1813 will be spun and developed. Copper stud bumps will be electro deposited on all the posts except constant posts. A thin layer of S1813 will be spun, baked, developed and constant bumps will be deposited. The remaining resist will be completely removed and PMMA will be cast on the wafer.

A printed circuit board will be fabricated on FR406 substrate. A test mask is being fabricated to check the feasibility of depositing 5µm square pads and 2µm wide traces on the circuit board. The wafer containing the integrated device will be bonded on the above printed circuit board. The silicon wafer will be completely etched and then the titanium and copper seed layer will be subsequently etched. Work is underway to optimize the electroplating parameters for fabricating copper and constantan stud bumps.

Figure 1: Device schematic of a section of the integrated array

Figure 2: Device setup
ACKNOWLEDGMENTS

This work is supported in part by a grant from Louisiana Board of Regents and by the department of Mechanical Engineering at LSU.

REFERENCES